DLC75R (.070" x .080")

◆DLC75R Capacitance & Rated Voltage Table

Cap.pF	Code	Tol.	Rated WVDC	Cap.pF	Code	Tol.	Rated WVDC	Cap.pF	Code	Tol.	Rated WVDC
1.0	1R0	B, C,D	500V Code 501	3.9	3R9	B, C,D	500V Code 501	22	220	G,J	500V Code 501
1.1	1R1			4.3	4R3			24	240		
1.2	1R2			4.7	4R7			27	270		
1.3	1R3			5.1	5R1			30	300		
1.4	1R4			5.6	5R6			33	330		
1.5	1R5			6.2	6R2			36	360		
1.6	1R6			6.8	6R8			39	390		
1.7	1R7			7.5	7R5			43	430		
1.8	1R8			8.2	8R2			47	470		
1.9	1R9			9.1	9R1			51	510		
2.0	2R0			10	100	G,J		56	560		
2.1	2R1			11	110			62	620		
2.2	2R2			12	120			68	680		
2.4	2R4			13	130			75	750		
2.7	2R7			15	150			82	820		
3.0	3R0			16	160			91	910		
3.3	3R3			18	180			100	101		
3.6	3R6			20	200						

Remark: special capacitance, tolerance and WVDC are available, consult with DALICAP.

◆Part Numbering

DLC75R 100 J W 501 T

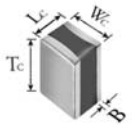
- Series
- Rated Capacitance* (See capacitance table)
- Capacitance Tolerance: (See capacitance table)
- Termination Type: Nickel,Plated 100%Sn(RoHS) Note:Laser marking is available on request.
- Rated Voltage
- Packaging Type: T:Tape carrier packaging 500pcs or 2000pcs/reel

* When capacitance is less than 1.0, use "R" for decimal

Code	A	B	C	D	F	G	J
Tolerance	±0.05pF	±0.1pF	±0.25pF	±0.5pF	±1%	±2%	±5%

◆DLC75R Chip Dimensions

unit:inch(millimeter)

Series	Term. Code	Type / Outlines	Capacitor Dimensions				Plated Material
			Length (L_C)	Width (W_C)	Thickness (T_C)	Overlap (B)	
DLC70R	W	 Chip	.070±.006 (1.78±0.15)	.080±.010 (2.03±0.25)	.120 (3.04) max	.200±.010 (0.50±0.25)	Sn/Ni (RoHS)

◆Design Kits

These capacitors are 100% RoHS. Kits contain 10(ten) pieces per value; number of values per kit varies, depending on case size and capacitance.

Kit	Description (pF)	Values (pF)	Tolerance
DKDLC75R01	1.0 - 3.6	1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8, 1.9, 2.0, 2.1, 2.2, 2.4, 2.7, 3.0, 3.3, 3.6	±0.10pF
DKDLC75R02	3.6 - 20	3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1	±0.10pF
		10, 11, 12, 13, 15, 16, 18, 20	±5%
DKDLC75R03	22 - 100	22, 24, 27, 30,33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91, 100	±5%

◆Performance

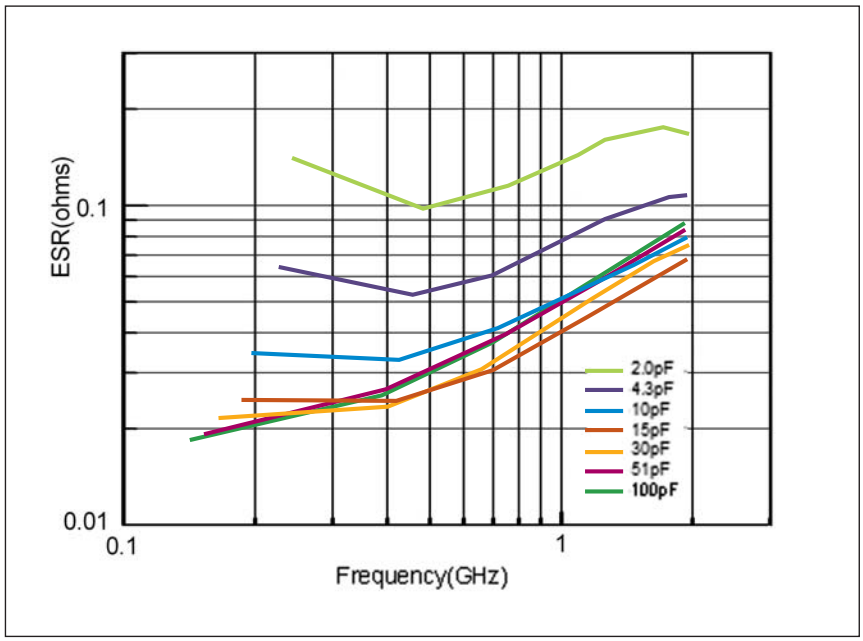
Item	Specifications
Quality Factor (Q)	2,000 min.
Insulation Resistance (IR)	10^5 Megohms min. @ +25℃ at rated WVDC. 10^4 Megohms min. @ +125℃ at rated WVDC.
Rated Voltage	500V
Dielectric Withstanding Voltage (DWV)	250% of rated voltage for 5 seconds.
Operating Temperature Range	−55℃ to +125℃
Temperature Coefficient (TC)	0±30ppm/℃
Capacitance Drift	±0.2% or ±0.05pF, whichever is greater.
Piezoelectric Effects	None

◆Environmental Tests

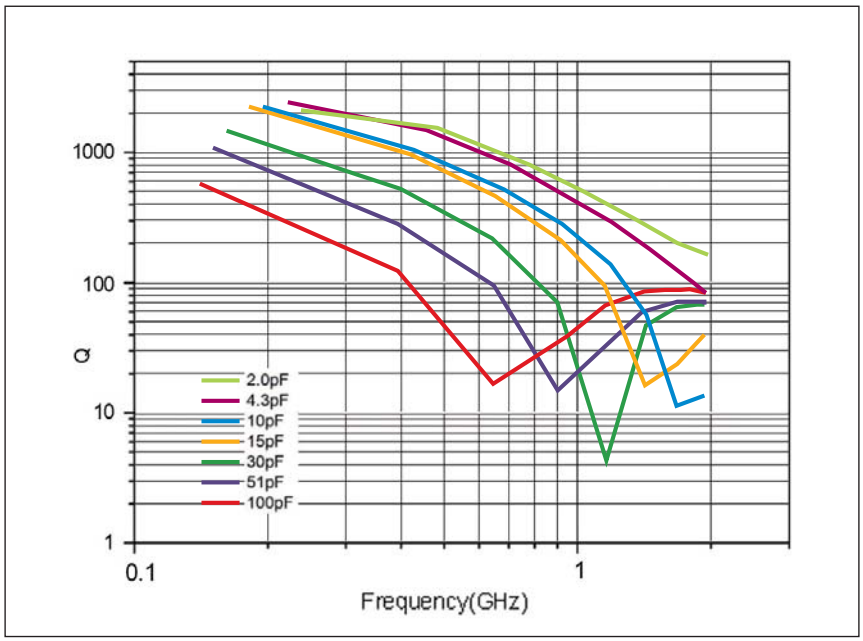
Item	Specifications	Method
Terminal Adhesion	Termination should not pull off. Ceramic should remain undamaged.	Linear pull force exerted on axial leads soldered to each terminal. 2.0lbs.
Resistance to soldering heat	No mechanical damage Capacitance change: −1.0% ~+2.0% Q>500 I.R. >10 G Ohms Breakdown voltage: 2.5 x WVDC	Preheat device to 150°C-180°C for 60 sec. Dip in 260°±5°C solder for 10±1 sec. Measure after 24±2 hours cooling period.
Thermal Shock	No mechanical damage Capacitance change:±0.5% or 0.5pF max Q>2000 I.R. >10 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 107, Condition A. At the maximum rated temperature stay 30 minutes. The time of removing shall not be more than 3 minutes. Perform the five cycles.
Humidity, Steady State	No mechanical damage Capacitance change: ±0.5% or 0.5pF max. Q>300 I.R. >1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 106.
Low Voltage Humidity	No mechanical damage Capacitance change: ±0.3% or 0.3pF max. Q>300 I.R. >1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 103, Condition A, with 1.5 Volts D.C. applied while subjected to an environment of 85°C with 85% relative humidity for 240 hours minimum.
Life	No mechanical damage Capacitance change: ±2.0% or 0.5pF max. Q>500 I.R. >1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 108, for 1000 hours, at the maximum rated temperature. 200% Rated voltage D.C. applied.

◆DLC75R Performance Curve

ESR vs Frequency

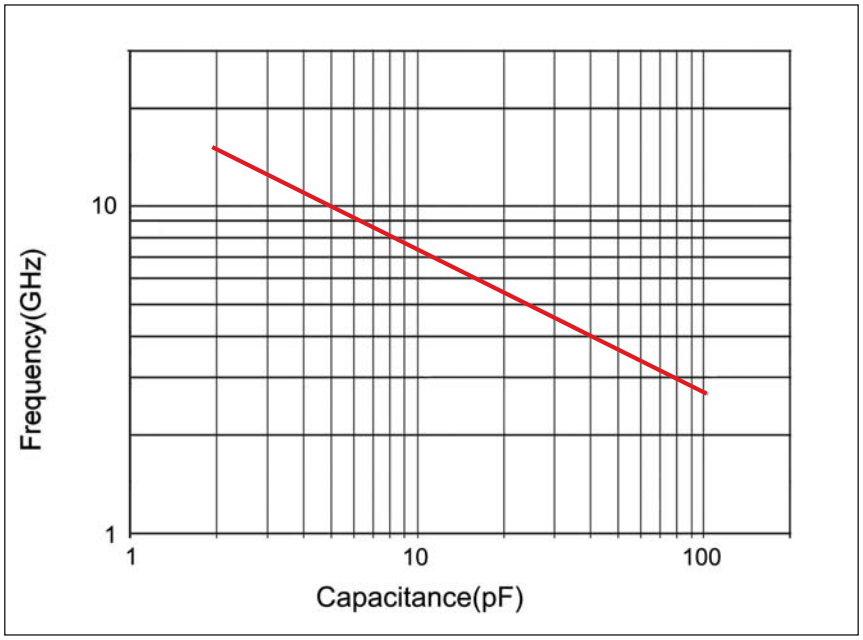


Q vs Frequency



◆DLC75R Performance Curve

First Parallel Resonant Frequency vs Capacitance



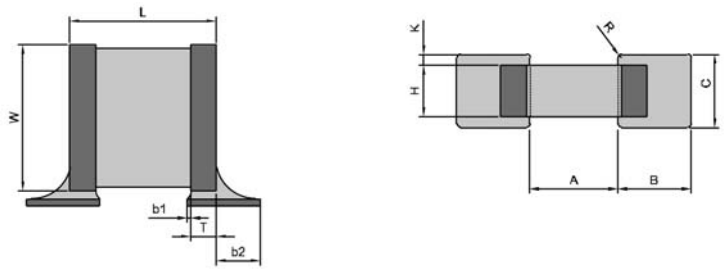
◆Recommended Land Pattern Dimensions

When mounting the capacitor to substrate, it's important to carefully consider that the amount of solder (size of fillet) used has a direct effect upon the capacitor once it's mounted.

1) The greater the amount of solder, the greater the stress to the elements. This may cause the substrate to break or crack.

2) In the situation where two or more devices are mounted onto a common land, be sure to separate the device into exclusive pads by using soldering resist.

Orientation	EIA	A	B	C
Vertical	0708	0.90	1.00	2.90



◆Tape & Reel Specifications

Orientation	EIA	A0	B0	K0	W	P0	P1	T	F	Qty/Min	Qty/reel	Tape Material
Vertical	0708	1.90	2.65	2.20	12.00	4.00	4.00	0.30	5.50	500	1500	Plastic