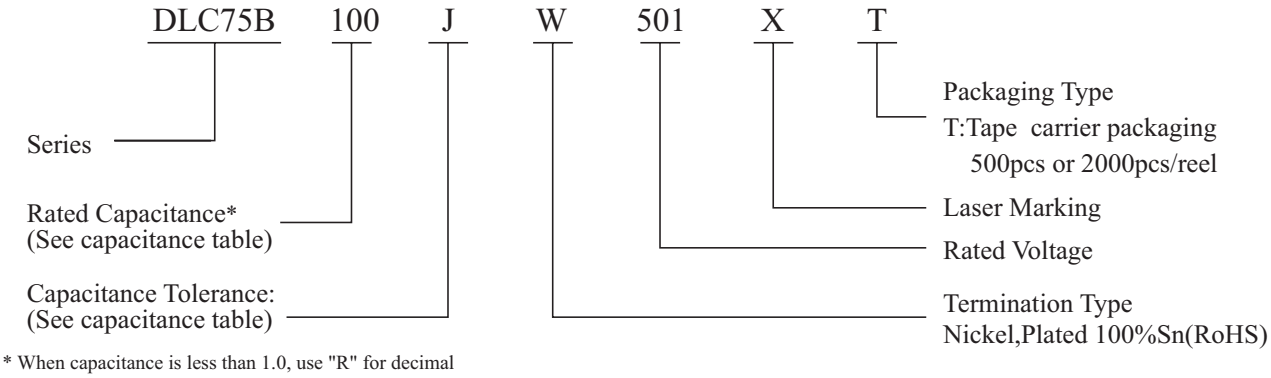
DLC75B (.110" x .110")

◆DLC75B Capacitance & Rated Voltage Table

Cap.pF	Code	Tol.	Rated WVDC	Cap.pF	Code	Tol.	Rated WVDC	Cap.pF	Code	Tol.	Rated WVDC	Cap.pF	Code	Tol.	Rated WVDC
0.2	0R2	A, B, C, D	500V Code 501 or 1000V Code 102	3.0	3R0	A, B, C, D	500V Code 501 or 1000V Code 102	27	270	F, G, J	500V Code 501 or 1000V Code 102	220	221	F, G, J	200V Code 201 or 500V Code 501
0.3	0R3			3.3	3R3			30	300			240	241		
0.4	0R4			3.6	3R6			33	330			270	271		
0.5	0R5			3.9	3R9			36	360			300	301		
0.6	0R6			4.3	4R3			39	390			330	331		
0.7	0R7			4.7	4R7			43	430			360	361		
0.8	0R8			5.1	5R1			47	470			390	391		
0.9	0R9			5.6	5R6			51	510			430	431	G, J	100V Code 101 500V Code 501
1.0	1R0			6.2	6R2			56	560			470	471		
1.1	1R1			6.8	6R8			62	620			510	511		
1.2	1R2			7.5	7R5			68	680			560	561		
1.3	1R3			8.2	8R2			75	750			620	621		
1.4	1R4			9.1	9R1			82	820			680	681		50V Code 500
1.5	1R5			10	100	F, G, J		91	910			750	751		
1.6	1R6			11	110			100	101		300 Code 301 or 600 Code 601	820	821		
1.7	1R7			12	120			110	111			910	911		
1.8	1R8			13	130			120	121			1000	102		
1.9	1R9			15	150			130	131						
2.0	2R0			16	160			150	151						
2.1	2R1			18	180			160	161						
2.2	2R2			20	200			180	181						
2.4	2R4			22	220			200	201						
2.7	2R7			24	240										

Remark: special capacitance, tolerance and WVDC are available, consult with DALICAP.

◆Part Numbering



* When capacitance is less than 1.0, use "R" for decimal

Code	A	B	C	D	F	G	J
Tolerance	±0.05pF	±0.1pF	±0.25pF	±0.5pF	±1%	±2%	±5%

◆DLC75B Chip Dimensions

unit:inch(millimeter)

Series	Term. Code	Type / Outlines	Capacitor Dimensions				Plated Material
			Length (L_C)	Width (W_C)	Thickness (T_C)	Overlap (B)	
DLC75B	W	 Chip	.110 +.020~−.010 (2.79+ +0.51~ −0.25)	.110 ±.010 (2.79 ±0.25)	.102 (2.60) max	.016 ~.039 (0.40~ 1.00)	Sn/Ni (RoHS)

◆Design Kits

These capacitors are 100% RoHS. Kits contain 10(ten) pieces per value; number of values per kit varies, depending on case size and capacitance.

Kit	Description (pF)	Values (pF)	Tolerance
DKDLC75B01	0.2 - 10	0.2, 0.5, 0.7, 0.8, 1.0, 1.2, 1.5, 1.8, 2.0, 2.4, 2.7, 3.0, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2	±0.10pF
DKDLC75B02	10 - 100	10	±5%
		10, 12, 15, 18, 20, 22, 24, 27, 30, 33, 39, 47, 56, 68, 82, 100	±5%
DKDLC75B03	100 - 1000	100, 120, 150, 180, 200, 220, 240, 270, 300, 390, 470, 560, 680, 820, 1000	±5%

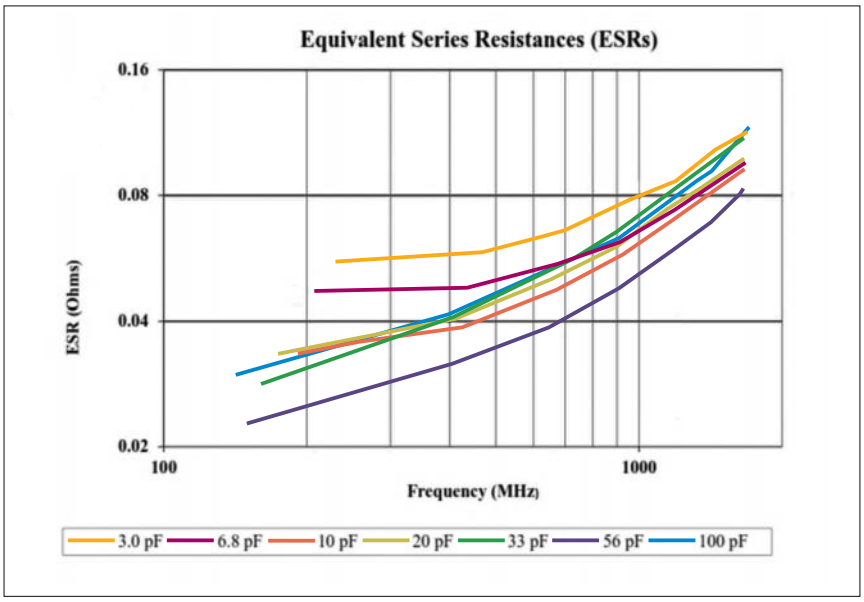
◆Performance

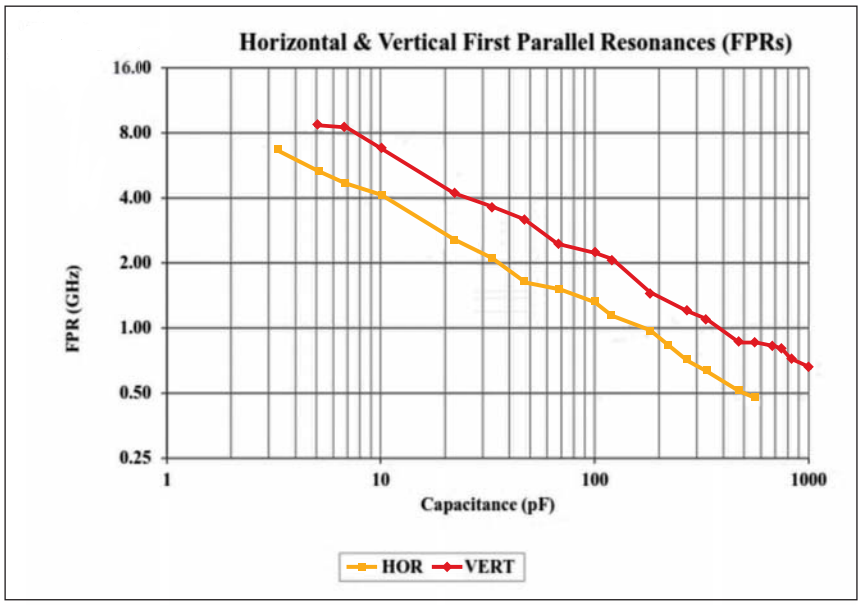
Item	Specifications
Quality Factor (Q)	2,000 min.
Insulation Resistance (IR)	10^5 Megohms min. @ +25℃ at rated WVDC.
Rated Voltage	See capacitance table
Dielectric Withstanding Voltage (DWV)	250% of Voltage for 5 seconds, Rated Voltage≤500VDC 150% of Voltage for 5 seconds, 500VDC< Rated Voltage≤1250VDC 120% of Voltage for 5 seconds, Rated Voltage>1250VDC
Operating Temperature Range	−55℃ to +125℃
Temperature Coefficient (TC)	0±30ppm/℃
Capacitance Drift	±0.2% or ±0.05pF, whichever is greater.
Piezoelectric Effects	None

◆Environmental Tests

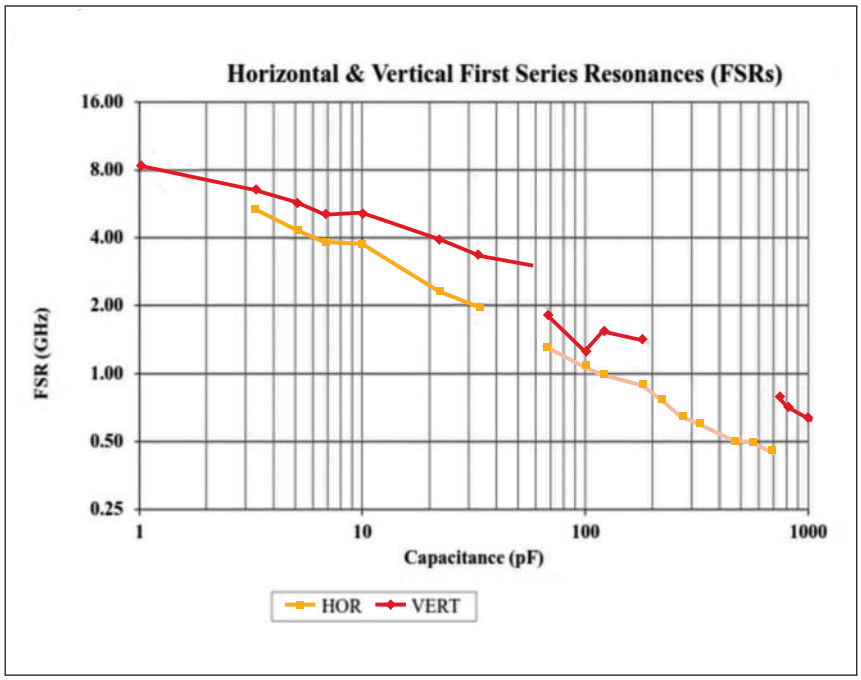
Item	Specifications	Method
Terminal Adhesion	Termination should not pull off. Ceramic should remain undamaged.	Linear pull force exerted on axial leads soldered to each terminal. 2.0lbs.
Resistance to soldering heat	No mechanical damage Capacitance change: −1.0% ~+2.0% Q>500 I.R. >10 G Ohms Breakdown voltage: 2.5 x WVDC	Preheat device to 150°C-180°C for 60 sec. Dip in 260°±5°C solder for 10±1 sec. Measure after 24±2 hours cooling period.
Thermal Shock	No mechanical damage Capacitance change:±0.5% or 0.5pF max Q>2000 I.R. >10 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 107, Condition A. At the maximum rated temperature stay 30 minutes. The time of removing shall not be more than 3 minutes. Perform the five cycles.
Humidity, Steady State	No mechanical damage Capacitance change: ±0.5% or 0.5pF max. Q>300 I.R. >1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 106.
Low Voltage Humidity	No mechanical damage Capacitance change: ±0.3% or 0.3pF max. Q>300 I.R. >1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 103, Condition A, with 1.5 Volts D.C. applied while subjected to an environment of 85°C with 85% relative humidity for 240 hours minimum.
Life	No mechanical damage Capacitance change: ±2.0% or 0.5pF max. Q>500 I.R. >1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 108, for 1000 hours, at 125°C. 200% of Voltage for Capacitors, Rated Voltage≤500VDC 120% of Voltage for Capacitors, 500VDC<Rated Voltage≤1250VDC 100% of Voltage for Capacitors,Rated Voltage>1250VDC

◆DLC75B Performance Curve





The First Parallel Resonance, FPR, is defined as the lowest frequency at which a suckout or notch appears in |S21|. It is generally independent of substrate thickness or dielectric constant, but does depend on capacitor orientation. A horizontal orientation means the capacitor electrode planes are parallel to the plane of the substrate; a vertical orientation means the electrode planes are perpendicular to the substrate.



The First Series Resonance, FSR, is defined as the lowest frequency at which the imaginary part of the input impedance, Im[Zin], equals zero. Should Im[Zin] or the real part of the input impedance, Re[Zin], not be monotonic with frequency at frequencies lower than those at which Im[Zin] = 0, the FSR shall be considered as undefined. FSR is dependent on internal capacitor structure; substrate thickness and dielectric constant; capacitor orientation, as defined alongside the FPR plot; and mounting pad dimensions.

Definitions and Measurement conditions:

The definitions on the charts are for a capacitor in a series configuration, i.e., mounted across a gap in a microstrip trace with a 50-Ohm termination. The measurement conditions are: substrate -- Rogers RO4350; substrate dielectric constant = 3.48; horizontal mount substrate thickness (mils) = 55; vertical mount substrate thickness (mils) = 45; gap in microstrip trace, horizontal or vertical mount (mils) = 61.1; horizontal mount microstrip trace width (mils) = 123.7; vertical mount microstrip trace width (mils) = 101.0. **Reference planes at sample edges.**

All data has been derived from electrical models created by Modelithics, Inc., a specialty vendor contracted by DLC. The models are derived from measurements on a large number of parts disposed on several different substrates.